**COMP 32211**

Two hours

**UNIVERSITY OF MANCHESTER**
**SCHOOL OF COMPUTER SCIENCE**

Implementing System-on-Chip Designs

Date: Friday 19th January 2018

Time: 09:45 - 11:45

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**Please answer all THREE Questions.**

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This is a CLOSED book examination

The use of electronic calculators is NOT permitted

**[PTO]**

1. a) In physical layout terms, what is the meaning of the word "standard" in a **standard cell**? (2 marks)

   b) In this (bad) Verilog example, in simulation, what will '`AA`' be after the next positive edge of '`clk`' if '`BB`' starts as 3 and '`CC`' starts as 5?

```
always @ (posedge clk) BB = CC;
always @ (posedge clk) AA = BB;
```

   (2 marks)

   c) Choose two distinct approaches to circuit **simulation** and outline where each may sensibly be used in SoC development. Justify this application in your answer. (One or two sentences for each is sufficient.) (2 marks)

   d) Briefly explain how – and why – the ***test patterns*** used in **production tests** may differ from those used in **design verification**. (2 marks)

   e) State two reasons why multiple *clock domains* may be necessary in an SoC design. (2 marks)

   f) What problem may appear when a data bus crosses a clock-domain boundary? How is this problem typically addressed? (2 marks)

   g) Briefly outline how a **scan chain** is used in production testing. (2 marks)

   h) '**Utilisation**' is an ASIC layout constraint which suggests how much of the available area should be used for the designers' logic cells. Why, on a modern ASIC, is this not set to 100%? (2 marks)

   i) Why is manufacturing **variability** such a problem in modern ASIC manufacture when it was only a minor concern 20 years ago? (2 marks)

   j) Reducing the supply voltage reduces both the speed and dynamic power dissipation of a CMOS circuit. Suggest how this observation might be exploited at the **design** stage of a computationally intensive SoC project. Mention any potential consequences of any changes which you suggest. (2 marks)

2. a) SoC architectures are moving away from being bus-based; interconnection is increasingly implemented using Network-on-Chip (NoC). What are the reasons for this? (4 marks)

b) Figure 1 shows a schematic symbol for a stage in an AXI-like connection. The `valid` signals indicate that there is data to transmit and the `ready` signals indicate there is space to accept data; both are acted on at the next active clock edge. Data transfer on a given interface (`in` or `out`) therefore occurs only under the condition: `ready AND valid`.

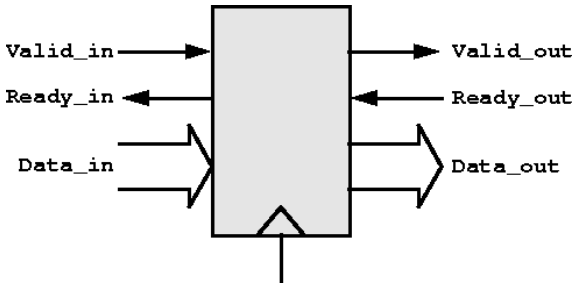


Figure 1: Data relay symbol

The stages are connected with a common clock with the assumption that all connected items are clocked *synchronously*. Suggest how such a clock can be distributed widely across the SoC. (2 marks)

c) Units such as the one depicted in figure 1 can be connected together (with no extra components) to carry data packets across a NoC. If each unit contains a single packet latch, why would it be impractical to achieve a throughput of one packet per clock cycle? What *is* the maximum throughput achievable? (4 marks)

d) Figure 2 shows a possible control state-diagram of the stage from figure 1. Transitions are labelled with the *actions* rather than the signal names; potential transitions which are not shown can be assumed to return to the current state.

Assume the reset state is state 'A'.

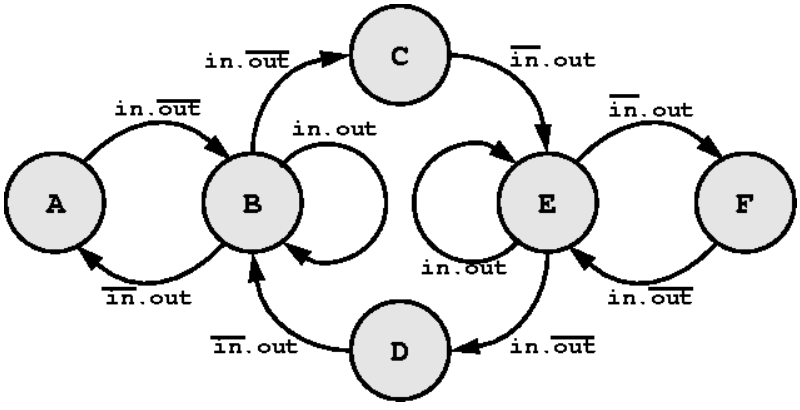


Figure 2: State diagram

For *each* of the six control states, indicate how many valid data packets are being held in the stage. (3 marks)

e) In which state(s) should the following output signals be asserted (true):

(i) `ready_in`?
(ii) `valid_out`?

In each case include a sentence explaining your reasoning. (2 marks)

f) Write some Verilog code which implements the state diagram in figure 2. You may assume that the state names {`'A`, `'B` etc.} are predefined, if you wish but use the actual signals – i.e. {`valid_in`, `ready_in`, `valid_out`, `ready_out`} – rather than the operations {`in`, `out`} in your code.

Minor syntactic errors will not be penalised but clear coding will be creditted. (5 marks)

3. a) What is meant by “leakage” in a CMOS transistor?
Why is any significant leakage a potential problem in an SoC? (2 marks)

b) What factor(s) affect(s) the amount of leakage contributed by any particular transistor? (2 marks)

c) In modern CMOS processes it is typical to have transistors with different ‘*threshold voltages*’ available. What effect(s) (if any!) does varying the threshold voltage have and where might the different transistors be used in a particular SoC design? (4 marks)

d) During logic synthesis it is usual to impose a *constraint* on the clock cycle time. What different delays does the synthesis tool need to fit within this constraint? (4 marks)

e) Assuming that the timing constraint is reasonably ‘challenging’ it is likely that the initial synthesis attempt will not meet it. What sort of tool will be used to estimate the performance and what is the principle of its operation? (2 marks)

f) Describe at least two distinct approaches which the synthesis tools could use to improve the circuit speed. (4 marks)

g) Why is it essential to run timing simulations again *after* performing place-and-route? (2 marks)


**END OF EXAMINATION**