COMP 32211

Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Implementing System-on-Chip Designs

Date: Monday 14th January 2019

Time: 09:45 - 11:45

Please answer all THREE Questions.

This is a CLOSED book examination

The use of electronic calculators is NOT permitted

[PTO]

1. a) Verilog allows the user to specify absolute delays in both circuits and simulations. These are not synthesised however. Why not? (2 marks)

   b) What is "**clock jitter**" and how might it be factored into the synthesis constraints? (2 marks)

   c) Briefly suggest how the **test coverage** desired during HDL design **verification** differs from that wanted for **production tests**. (2 marks)

   d) Define the **hold time** of a D-type flip-flop. In the flip-flop circuit shown in figure 1, what *constraint(s)* are there on the hold time of flip-flop A? (2 marks)

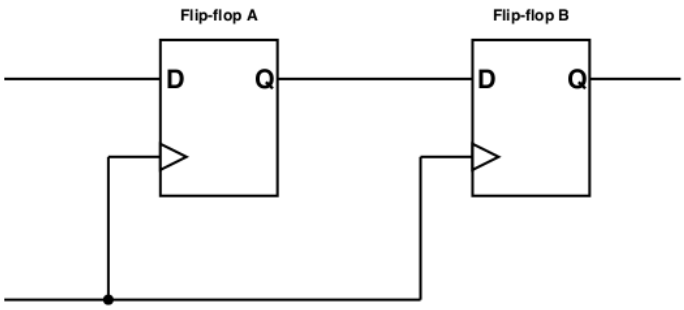


Figure 1: Flip-flops

   e) The Verilog code given in figure 2 specifies a combinatorial multiplexer/selector circuit with three legitimate outputs. What is the reason for the '`default`' statement and what would a logic synthesizer do if it were omitted? (2 marks)

```
case (select)
  2'h0: Q = input_0;
  2'h1: Q = input_1;
  2'h2: Q = 16'hFFFF;
  default: Q = 16'hxxxx;
endcase
```

Figure 2: Verilog case statement

   f) What factors affect the *dynamic* power dissipation in a CMOS subcircuit? (List all that you can think of.)
   Which might be regarded as the most important for a design engineer to address, and why? (2 marks)

   g) Outline some problems for ASIC manufacturers which are increasing due to 'Moore's Law' device shrinkage. (2 marks)

h) Explain what is meant by “regression testing”. (2 marks)

i) Write Verilog code for positive-edge triggered D-type flip-flops:

i) with a synchronous clear

ii) with an asynchronous clear and an enable

clearly identifying which is which. (2 marks)

j) In terms of ASIC layout, what is a “**macrocell**”? Give an example. (2 marks)

2. a) Figure 3 shows a transistor-level schematic of a standard cell. Derive a truth table for this circuit and write a Verilog `assign` statement which performs an equivalent function. (3 marks)

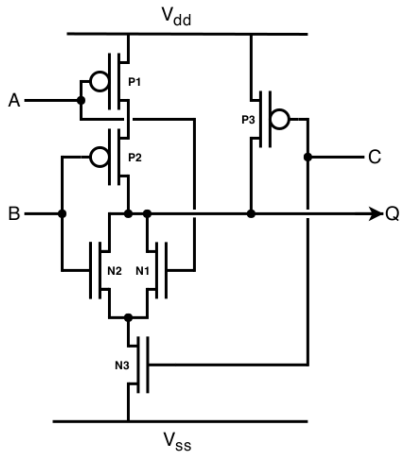


Figure 3: Transistor circuit

b) How does the **width** of a MOSFET affect its output impedance/'drive'? (1 mark)

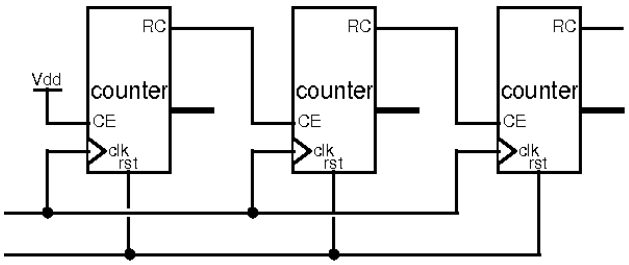
c) Assuming the same *carrier mobility* in the PMOS and NMOS transistors, should any of the transistors be differently sized to balance the 'drive strength' of the circuit in fig. 3? Justify your answer. (2 marks)

d) On an ASIC, some gate outputs connect only to other, close-by cells. However if a signal needs to be transmitted a 'long distance' on a chip what extra problems become significant? (4 marks)

e) How do ASIC CAD tools try to alleviate any of the problems you have identified with 'long-distance' signal transmission on a chip? (4 marks)

f) An ASIC is being designed for a new *Smartwatch*. The target process allows two different threshold transistor families. When the Verilog is first synthesized, the tools report that 40% of the standard cells use low V_t transistors and 60% use high V_t transistors. Your manager seems unhappy with this: what can you do to improve the ASIC design? (6 marks)

3. Figure 4 shows a design for a modulo 1000 counter, using a Verilog module instantiated on a schematic. *This design has not yet been debugged!*




```
module counter(input wire clk,
               input wire CE,
               input wire rst,
               output reg [3:0] count;
               output reg RC)

always @ (posedge clk)
if (rst) count <= 0;
else
  if (CE)
    if (count == 9) count <= #1 0;
    else count <= #1 count + 1;
  else count <= #1 count;          // AA

always @ (posedge clk)
if (rst) RC <= #1 0;
else     RC <= #1 (count == 9);

endmodule
```

Figure 4: A *putative* modulo 1000 counter.

a) For a single '`counter`' only, sketch a timing diagram of a test simulation run you might use to verify the module. (Include the module outputs in the trace.) (3 marks)

b) The symbol '#1' appears several times in the Verilog code. What effect does this have on:

(i) the behavioural simulation?

(ii) a subsequently synthesized circuit? (2 marks)

c) Is the reset ('`rst`') action within the module '`counter`' synchronous or asynchronous? Justify your answer. (1 mark)

d) Considering the design as a whole, is the modulo 1000 counter synchronous or asynchronous? Again, justify your answer. (1 mark)

e) The designer's intent is that the whole design repeatedly cycles though successive binary-coded decimal (BCD) outputs from `000` to `999`.
There are functional bugs in the Verilog and in the schematic. Identify these bugs and suggest appropriate ways in which they could be corrected. (8 marks)

f) The '`RC`' output from the '`counter`' module, as written in figure 4 is *registered*, i.e. the output comes directly from a flip-flop. Identify one advantage and one disadvantage of this style of design. (4 marks)

g) Is the line in the Verilog which is marked with the comment '`AA`' necessary? Why, or why not? (1 mark)

END OF EXAMINATION