1 hr 30 mins

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Implementing System-on-Chip Designs

2020/21

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Answer all questions

1. (a) While testing your designs, sometimes you may get 'X' and 'Z' states in the outputs in the Verilog simulation trace. What is the meaning of each of these two states? What important information you could rationally infer from such output states? [3 marks]

   (b) You can add absolute delays (e.g. #3) in the Verilog description of your module. How these delays are handled by synthesis tools? Explain the purpose of adding such absolute delays? [5 marks]

   (c) Consider the following (bad) Verilog example code (this code will be synthesised although it is a bad practice to write code in this way). What will be the final value of 'XX', 'YY' and 'WW' after the next positive edge of 'clk'? Assume that initially, XX is holding decimal value '10' and ZZ is holding decimal value '12'. [6 marks]

```
always @ (posedge clk) XX = ZZ;
always @ (posedge clk) YY = XX;
always @ (posedge clk) WW <= XX;
```

   (d) Consider the given the following Verilog *'always'* block:

```
always @ (negedge clk)
begin
#2;
x <= #3 x - 1;
#4;
y <= #5 x + 1;
end
```

   Assume that initially, the variable 'x' is holding a decimal value 10 and 'clk' makes a transition from high to low at time '15'. What will be the final values in variables 'x' and 'y' and what will be the simulated time when these variable are updated? [6 marks] (20 marks)

2. (a) The term "threshold voltage" can be interpreted in two different ways in the context of a digital electronic circuit. Name and explain each of the interpretations briefly. [6 marks]

   (a) The logic gates can be constructed with transistors having 'low' and 'high' thresholds and both types of transistors can be used on a single SoC. Assume that you are designing an SoC and reducing power consumption is the main design goal. Which type of transistors you will prefer in your logic gates and why? [6 marks]

   (a) Consider CMOS transistors based circuit as shown in Figure 1. It has two inputs 'A' and 'B' and one output 'F'. Write down the truth table and the Boolean expression for the output 'F'. Also, name the logical gate being implemented by this circuit. [8 marks]

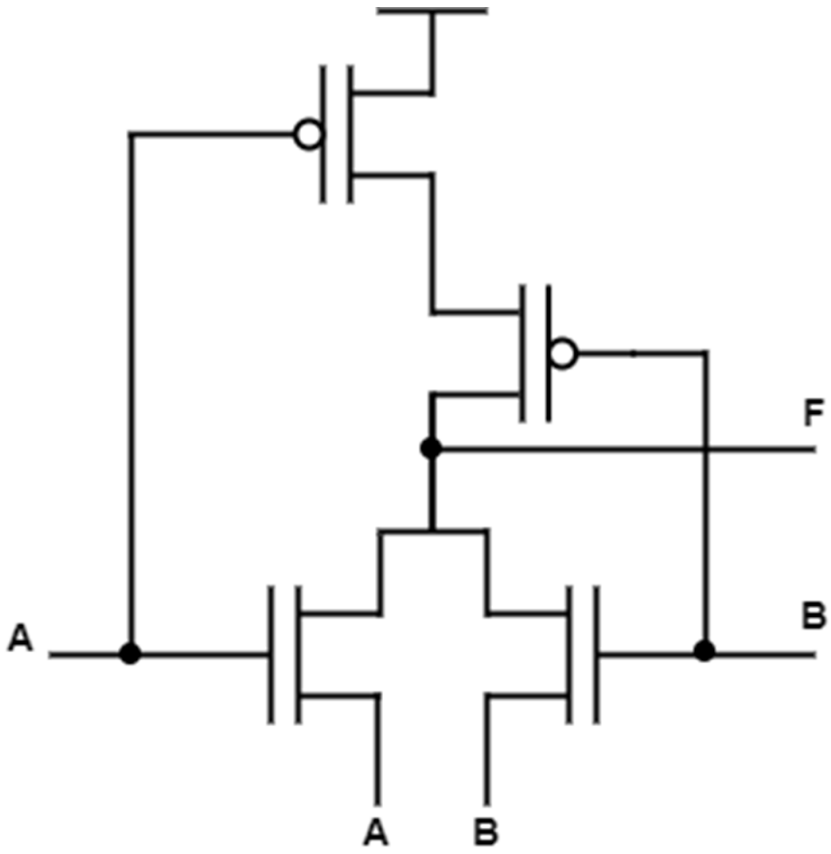

Figure 1: CMOS transistors based circuit

(20 marks)

3. Consider interconnection of two clocked domains as shown in Figure 2. The combinatorial logic responsible for the decision making is hidden within the logic 'clouds'. The 'sync. logic' sub-block is responsible for the synchronisation between these two clock domains

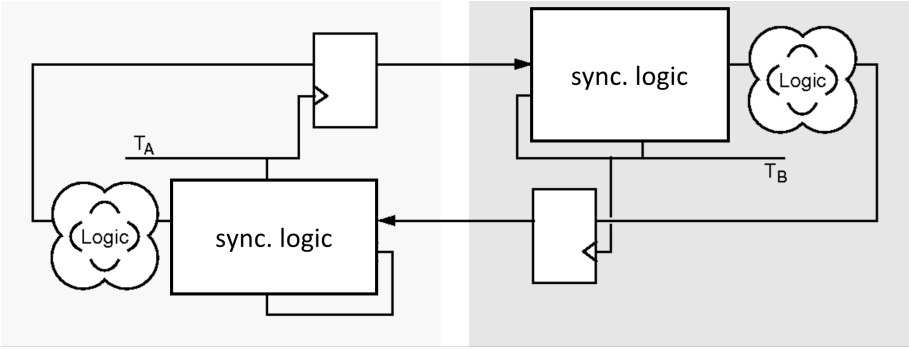

Figure 2: Interconnection of two independent clock domains

(a) What is the purpose of these 'sync. logic' blocks as shown in Figure 2? Explain what would happen if the 'sync. logic' sub-blocks are removed from both clock domains. [4 marks]

(a) Explain two techniques that can be used to design the 'sync. logic' sub-blocks as shown in Figure 2. [6 marks]

(10 marks)

END OF EXAMINATION