Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Implementing System-on-Chip Designs

January 2022

Time: Whenever

Please answer everything.

The use of electronic calculators is not permitted.

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1. a) What is meant by "SIMD"? Give an example where this is used in modern systems-on-chip with a (one sentence) justification of why this is appropriate. (2 marks)

   b) In which order and at what times should the following signals {`aaa, bbb, ccc, ddd`} change (if they do) relative to the active clock edge? Assume no other events are pending and the other inputs are static. (2 marks)

```
always @ (posedge clk)
  begin
  aaa <= #10 input_1;
  bbb <=     input_2;
  end

always @ (*)
  begin
  #10 ccc = aaa;
      ddd = bbb;
  end
```

   c) What is "power gating" on an SoC? What would be a *disadvantage* of using this on an entire microcontroller subsystem in an SoC? (2 marks)

   d) A graphics display for a portable device has a visible display resolution of 1000×800 pixels with an additional total of a 25% overhead spent in the blanking period. The pixels use '32-bit colour' and the screen refreshes at 50 Hz.
   How much *memory bandwidth* (in bytes/s or Mbytes/s) is needed to maintain this display?
   For the purpose of this question, ignore any other memory accesses; in the absence of calculators an approximate answer is acceptable. (2 marks)

   e) In a Verilog 'behavioural' simulation the value '`x`' on a signal or bus can mean slightly different things. What is signified by this: (2 marks)

      (i) when specified as a value in a module – e.g. in the '`default`' in a '`case`' statement?

      (ii) at the output of a register or flip-flop during simulation?

   f) What is the effect of increasing the *width* of a MOSFET and when might this be used in a VLSI design? (2 marks)

   g) Give an example of an ASIC tool or process performed after the place-and-route has been done, other than more simulation. Briefly say why this step is necessary. (2 marks)

h) Given that "*verification*" is the process used to ensure a design fulfils its required specification whilst "*test*" is a post-production process applied to every manufactured VLSI chip, what are the basic differences applied to the design of the *test patterns* used for each and why are these appropriate? (2 marks)

i) In digital electronics, give two distinct meanings of the term "threshold voltage". (2 marks)

j) Explain why Advanced Periheral Bus (APB) model cannot be utilised in a burst mode to make multiple transfers? Also briefly describe under what circumstances APB is still useful. (2 marks)

2. a) Give three reasons why most modern FPGA designs use *synchronous* clocking across one or more of their subsystems. (6 marks)

   b) What is 'clock skew' and how is it kept within manageable bounds in a chip design? (2 marks)

   c) When timing a logic pipeline, what is meant by "balance"? (1 mark)

   d) A computer architect laying out a logic pipeline has a problem: a memory macrocell block has a critical path which is both longer than those of its neighbours and longer than the desired clock period. What can be done to alleviate this problem and attain the desired throughput? Explain how your proposal would solve the problem. (4 marks)

   e) Figure 1 shows two proposed designs for a unit where the register captures FSM output on every *third* clock cycle. Briefly outline any advantages and disadvantages you can see in each proposal. Which would you choose for an FPGA implementation, and why? (5 marks)

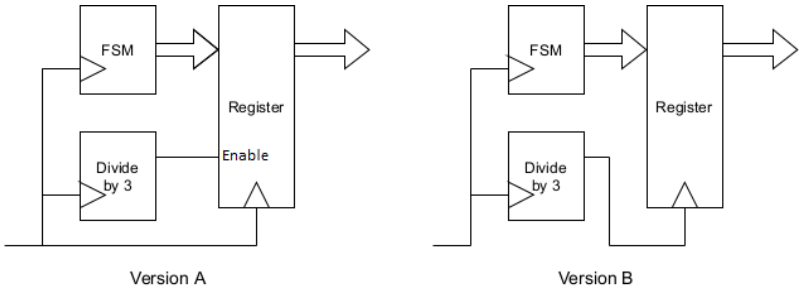

Figure 1: Alternative sequential logic designs

   f) A wrist watch is typically clocked from an oscillator running at 32768 Hz. (Hint: this is 2^{15} Hz.) This is divided down with a *ripple counter* – i.e. one where the output of each flip-flop is clocked from the *data* output of its predecessor: see figure 2 for detail. Why do the designers do it this way? (2 marks)

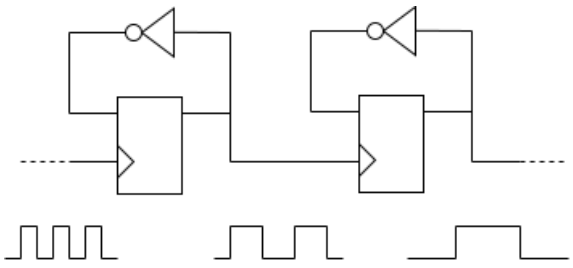

Figure 2: Ripple counter detail

3. a) As an ASIC designer, you have been given the task of designing a logic circuit and optimising the propagation delay. Assuming that the target process allows two different threshold transistor families, which type of transistors you will prefer in your design and why? What could be the drawback of using such transistors? (5 marks)

   b) Consider a CMOS transistors based circuit as shown in figure 3. It has two inputs 'A' and 'B' and one output 'Out'. Write down the truth table and the Boolean expression for the output 'Out'. Also, name the logical gate being implemented by this circuit. (6 marks)

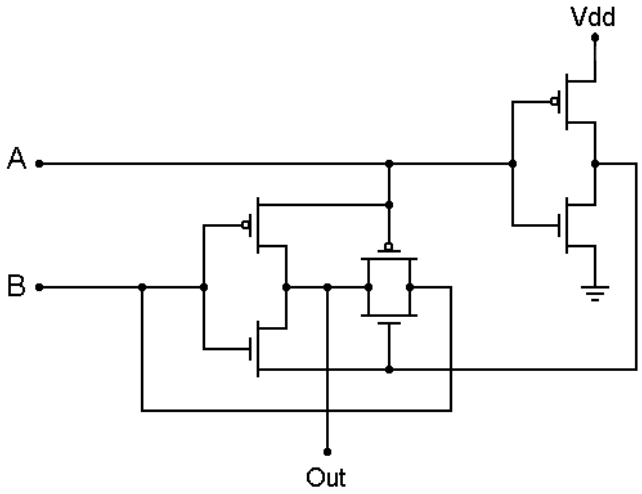

Figure 3: CMOS transistor-based circuit

   c) Consider a synchronous AXI-like stage as shown in figure 4. The main aim of such logic is to receive and transmit data on every clock cycle to improve overall throughput. Assuming that it has only one internal buffer, explain under what conditions data is received and transmitted by such AXI-like stages. (4 marks)

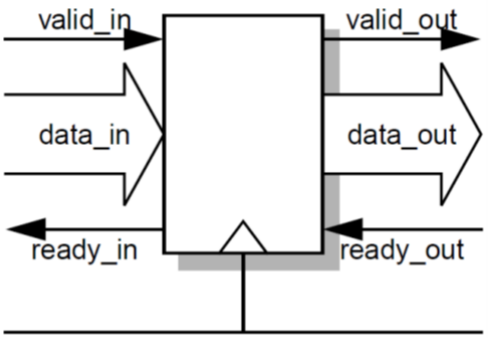

Figure 4: AXI-like stage

   d) Explain why bus-based communication architectures are becoming impractical to use in modern SoC designs. What could be the alternate solution and describe how AXI-like stages (such as shown in figure 4) can be customised and utilized for that purpose? (5 marks)

END OF EXAMINATION