COMP32211

Two Hours

UNIVERSITY OF MANCHESTER

IMPLEMENTING SYSTEM-ON-CHIP DESIGNS

24 January 2023

14:00 – 16:00

Please answer ALL of the questions provided

Use a SEPARATE answerbook for each SECTION.

For full marks your answers should be concise as well as accurate.
Marks will be awarded for reasoning and method as well as being correct.
Total marks = 60.

The use of electronic calculators is NOT permitted

1. a) In Verilog, a value may be specified in the form `32'hxxxxxxxx`; this can have different meanings. Explain how such a value might be used:
   i) to assist with verification by simulation.
   ii) to provide freedom for optimisation during synthesis. (2 marks)

   b) In a block of Verilog source code *intended for synthesis*, why is it highly undesirable to write "`always @ (posedge signal)`" when '`signal`' is not the clock? Give at least *two* different reasons. (2 marks)

   c) You are tasked to implement a custom computing accelerator to perform high-speed matrix multiplication. (Matrix multiplication involves successive, near-consecutive multiply/accumulate operations, in case you have forgotten!) Outline a suitable architecture for the arithmetic computation unit and include a *brief* justification of your choice of approach. (2 marks)

   d) What is the principle behind 'Monte Carlo' testing? Give one advantage and one disadvantage of such tests. (2 marks)

   e) Various CAD tools can be used to assist design verification. When employing an automated *test coverage tool*, give *two* examples of the types of potential oversight in verification it can detect, and *two* examples of types of mistake it would not find. (2 marks)

   f) What effects result from lowering the 'transistor threshold' (V_t) in a CMOS gate? (2 marks)

   g) Why does reducing the clock frequency reduce the power consumed by a CMOS circuit? Why does it (slightly) *increase* the *energy* needed to complete a computing operation? (2 marks)

   h) Briefly describe 'leakage' in a MOS transistor. (2 marks)

   i) For systems off-chip communication, usually *serial* interface is preferred. Why is that? Also list at least two serial interfaces being used for that purpose. (2 marks)

   j) Briefly explain the importance of 'Buffer inseration' in ASIC design flow. In general, at what stage or process of the ASIC design flow this step is performed? (2 marks)

2. a) Give three distinct reasons why a system-on-chip might be divided into multiple *clock domains*. (3 marks)

   b) Why, *in the general case*, can the transfer of data between clock domains not be made 100% reliable? (2 marks)

   c) How is the clock resynchronisation when crossing timing boundaries typically addressed to reduce failure rates to acceptable bounds (in the general case)? (2 marks)

   d) The problems encountered in the previous parts of the question can be eliminated under some *particular* circumstances; what constraints would be required to ensure this? (3 marks)

   e) You are tasked to design an interface between two units which are clocked from independent sources. The data transfer is a one-way flow of packets, sometimes being quite widely spaced in time and sometimes coming in rapid bursts. (The overall pattern is not predictable.)
   Outline a design which can provide high transfer *bandwidth* for the bursts whilst not imposing significant extra *latency* on the single transfers (over the burst latency). (8 marks)

   f) Assuming, in the previous question part, that packets always contain 4 bytes of data and the datapath allows the transfer of one packet per clock, what is the *maximum* data transfer rate in byte/s if the transmitter is clocked at 300 MHz and the receiver at 240 MHz? (2 marks)

3. a) A schematic of a standard cell using CMOS transistors is shown in figure 1. Drive the truth table and the Boolean expression for the output 'F_out'. Also, name the combinatorial logic being implemented by this cricuit. (7 marks)

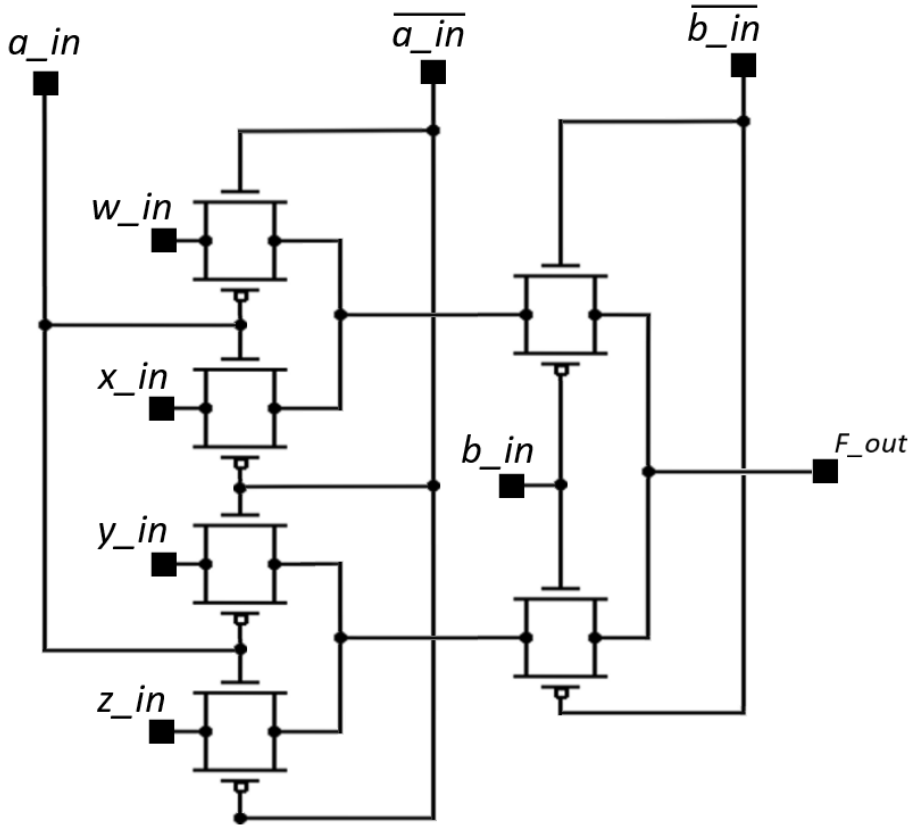

Figure 1: Transistor-level circuit

b) The standard cell illustrated in figure 1 has been designed using a logic gate consisting of two CMOS transistors . What is this logic gate, also shown in figure 2, called in general? Explain its working and under what conditions it is preferred by the designers? Also, give some examples of other standard cells that can be made using this logic gate. (5 marks)

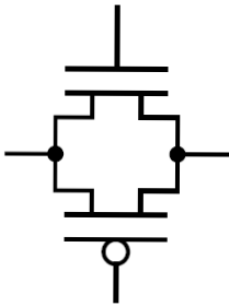

Figure 2: Logic gate

c) Three interconnecting logic domains from an SoC are shown in figure 3. Considering each domain is connected to different supply voltage by design ($V_{dd-1} = 1.2V, V_{dd-2} = 1.0V, V_{dd-3} = 0.8V$), briefly answer the following questions

- Explain the purpose of PMOS transistor connected to the voltage supply V_{dd-1}? (2 marks)
- What role does the threshold voltage (V_{th}) of PMOS transistor play in operation of this circuit? (1 mark)
- What would happen if you replace this PMOS transistor with a NMOS transistor? (1 mark)
- What is the benefit(s) (if any) of having multiple voltage supplies in this SoC? (2 marks)
- What extra logic should be included (if required) within each domain to pass signals among themselves and why? (2 marks)

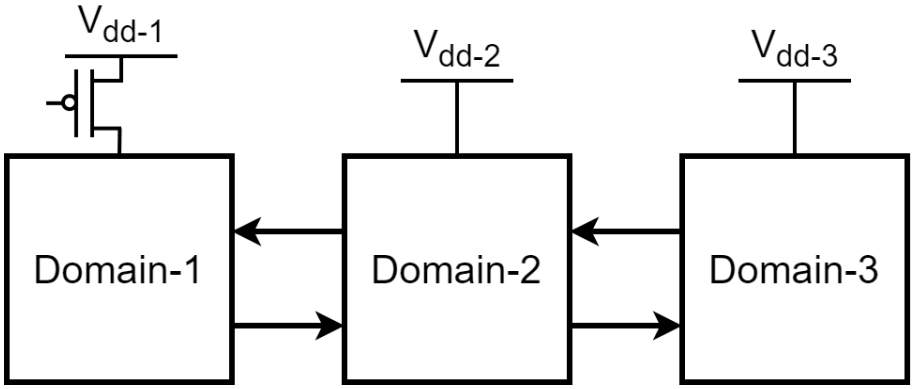

Figure 3: Block-level SoC design

END OF EXAMINATION