Two hours

UNIVERSITY OF MANCHESTER

Implementing System-on-Chip Designs

15 January 2024

14:00 - 16:00

Please answer everything.
Use a SEPARATE answerbook for each SECTION.
For full marks your answers should be concise as well as accurate.
Marks will be awarded for reasoning and method as well as being correct.
Total marks = 60.

The use of electronic calculators is not permitted.

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1. a) What is meant by "regression testing"? Give two *principles* which, if observed, contribute to the operation of an efficient regression test.
(By 'principles' we mean general things such as appropriate design choices.)
(2 marks)

b) What is meant by 'memory interleaving'? Briefly describe how this might be used to 'share' the same memory between (for example) a processor's instruction and data buses. (2 marks)

c) You are tasked to produce a digital module which has to evaluate 32×32-bit integer multiplications. These are needed rapidly (low latency) but only occasionally (low bandwidth). Suggest an appropriate *architecture* giving a justification as to why it might be applicable. (2 marks)

d) Why is controlling and minimising *clock skew* important in modern digital circuits? (2 marks)

e) Verilog has two types of digital comparison operator, as typified by "==" and "===". How do these differ when used in the general language (i.e. simulation) and are there differences in the circuits synthesized from each? (2 marks)

f) What process is typically performed immediately after completing the electrical rules checks (ERC) in ASIC design? Briefly explain why that process is necessary. (2 marks)

g) What are the effects of raising the 'transistor threshold' (V_t) in a CMOS gate? (2 marks)

h) How do manufacturing variations typically impact the properties of PMOS and NMOS transistors in semiconductor devices? (2 marks)

i) Briefly explain how current is conducted in an n-channel (NMOS) transistor, and why? (2 marks)

j) Briefly discuss the limitations that prevent the use of the Advanced Peripheral Bus (APB) model for burst mode transfers. In what situations is APB still a good choice? (2 marks)

2. Here is a section of Verilog source code which defines a four-entry data FIFO.

```
module buffer(input  wire       clk,         // Clock
input  wire       reset,       // Reset
input  wire       in_en,       // Input interface
input  wire [7:0] data_in,
output reg        full,
input  wire       out_en,      // Output interface
output wire [7:0] data_out
output wire       empty);

reg  [7:0] storage [0:3];                    // Data storage
reg  [1:0] head, tail;                       // Pointers
reg  [1:0] next_tail;                        // Modulo 2 bits

always @ (tail) next_tail = tail + 2'h1;

always @ (posedge clk)
if (reset) tail <= #2 2'h0;
else if (in_en)
begin
tail <= #2 tail + next_tail;
storage[tail] <= #2 data_in;
end

assign data_out = storage[head];

always @ (posedge clk)
if (reset) head <= #2 2'h0;
else if (out_en) head <= #2 head + 2'h1;

always @ (posedge clk)
if (reset) full <= #2 1'b0;
else full <= #2 (!out_en && (full || (in_en && (next_tail == head))));

assign empty = ???????                       // For completion below

endmodule
```

Assume the environment is 'well behaved' so it will never produce an `in_en` when the FIFO indicates it's 'full' nor an `out_en` when there is no data to read (i.e. the output status is currently indicating `empty`).

a) Sketch a **state diagram** of the device. Indicate on the figure how the control outputs {`empty`, `full`} are derived. (4 marks)

b) Explain why the '`full`' *flip-flop* is necessary. (2 marks)

c) Derive appropriate logic to derive the (active high) '`empty`' signal to replace the '`???????`' in the example. (As the name might suggest, its purpose is to indicate that the FIFO holds no valid data.) If you need to *change* other existing code – such as the declaration – please indicate that in your answer. Minor syntactic deviations will not be penalised. (4 marks)

The circuit is being verified with a simulation test bench. Assume:

- The clock (`clk`) has rising edges every 10 units (at times 10, 20 etc.); we begin this analysis at time 101.
- A reset sequence has already taken place (and will not recur).
- `in_en` and `out_en` have been inactive (low) from time 0, throughout the device reset.

d) What are the expected output states of the signals `empty`, `full` and `data_out` at time 101? (2 marks)

e) At time 101 `data_in` is set to `8'h5A` and `in_en` is raised to 'active' (i.e. '`1'b1`'). Time is then allowed to advance to 115. List the signal changes to both internal registers and all output signals over this period, including:

- The *time* that the change actually occurs in the simulation.
- The *order* of changes when they occur at the same time as determined by the Verilog simulator.

If ordering is not determinable, also make that clear in your description.

(8 marks)

3. a) A schematic of a standard cell using CMOS transistors is shown in figure 1. Drive the truth table and the Boolean expression for the output 'F_out'. Also, name the combinatorial logic being implemented by this cricuit. (7 marks)

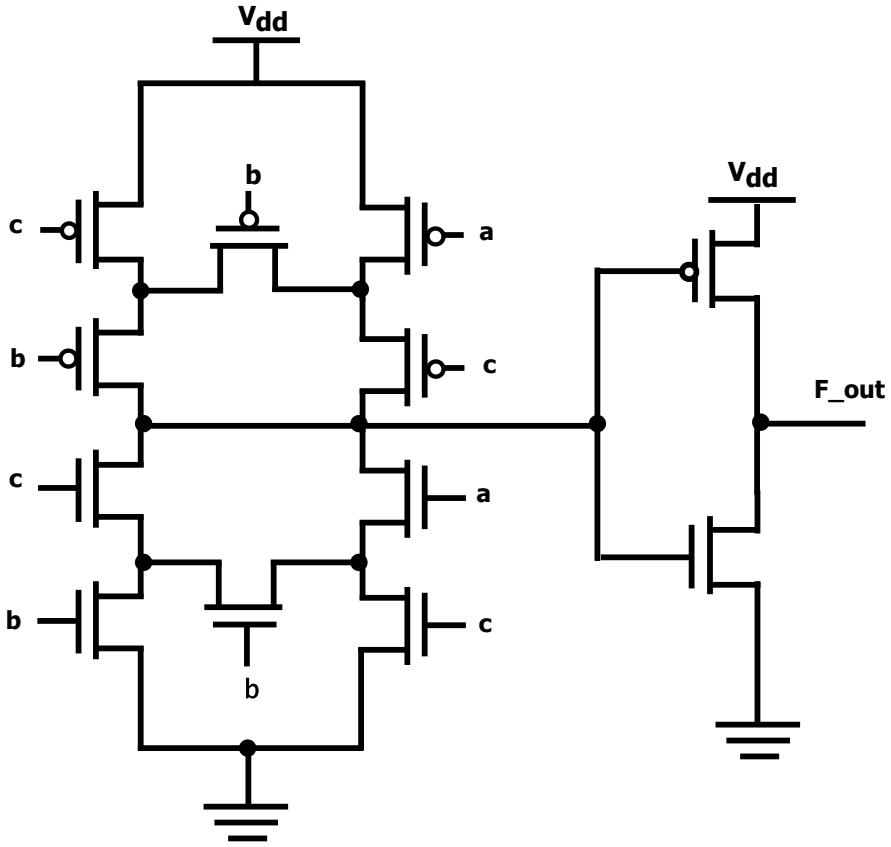

Figure 1: Transistor-level circuit

b) Define a "macrocell" in the context of ASIC layout. Explain how macrocells differ from standard cells. Provide examples of situations where using macrocells can be advantageous in integrated circuit design. Which particular process within the ASIC design flow handles the placement of macrocells? (6 marks)

c) Consider a synchronous AXI-like pipeline as shown in Figure 2.

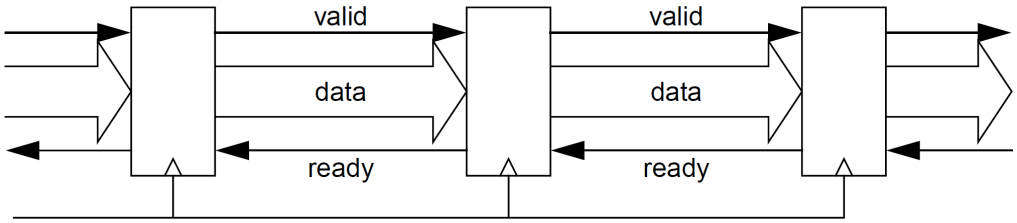

Figure 2: AXI-like pipeline

- What is the purpose and main benefit of this AXI-like pipeline? (1 mark)

- Explain the basic working of the protocol for reading/writing data from one stage to another stage in this AXI-like pipeline, particularly focusing on the 'valid' and 'ready' signals. (2 marks)

- How can each stage of this AXI-like pipeline be optimised to ensure optimal performance? (1 mark)

- Why are traditional bus-based communication architectures facing challenges in modern SoC designs, and what alternative solutions can address these issues? (3 marks)

END OF EXAMINATION