Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Implementing System-on-Chip Designs

January 2025

Time: Whenever

Please answer everything.

The use of electronic calculators is not permitted.

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1. a) The following code fragment is legitimate Verilog, but it will cause problems if synthesized. What is the problem and how might you fix it? (2 marks)

```
always @ (select, first, second)
casex (select)
  2'b0x: result = first;
  2'b10: result = second;
endcase
```

b) In the context of ASIC/SoC development, what is typically referred to as a 'buffer':

i. in layout when connecting standard cells.

ii. on a datapath between communicating functional blocks.

In each case include a sentence outlining their purpose. (2 marks)

c) In an ASIC process you have 'high-V_{th}' and 'low-V_{th}' CMOS transistor gates available: what is the chief advantage of each over the other?
Which should be chosen for a 'non-critical path'? (2 marks)

d) What logic function does the transistor circuit in figure 1 implement? (2 marks)

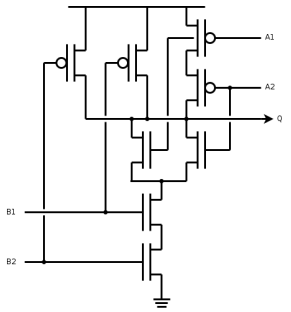

Figure 1: Mystery complex gate

e) How can a 'test coverage tool' improve confidence in the verification of a HDL circuit design? Why developing tests using such tools typically *iterative*? (2 marks)

f) Briefly describe an aspect of *functional* test coverage which may ***not*** be detected with test coverage tools, even if they report '100% coverage'. (2 marks)

g) When simulating a clock cycle time during ASIC modelling it is important to allow for variation in **PVT**; Why is that and what do these letters stand for? (2 marks)

h) What is 'Monte Carlo' testing? What contribution can it make to a verification process? (2 marks)

i) Figure 2 shows a buffer comprising two inverters running from potentially different power rails $\{V_{dd}1, V_{dd}2\}$. This is satisfactory under some circumstances but has a problem with a particular relationship of the supplies. What is the problem and under which circumstance does it occur? (2 marks)

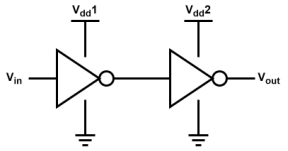

Figure 2: Domain crossing

j) An interface transfers a 32-bit value ('`value`') at a rising edge of a clock ('`clk`') when validated by an active-high control signal ('`valid`'). Write a Verilog statement for a testbench which would produce and output an **event** ('`oops`') if the value was not defined when a transfer was indicated. (2 marks)

2. a) In VLSI layout, what are the general physical characteristics of 'standard cells' and 'macrocells'? (4 marks)

   According to need, on chip storage may be implemented in D-type **registers** or in blocks of **SRAM**.

   b) For each of these components, state whether their basic components would be standard cells or macrocells. (2 marks)

   c) State and contrast two characteristics of the implementations of these types of storage which would influence the choice of one or the other in an RTL design. (4 marks)

   d) From the previous question part, give an appropriate example of the *use* of *each* type of storage as **components** on an SoC *other than the processor register and memory/cache applications.* (4 marks)

   Transistors in SRAM cells (fig. 3) are made as small as possible: the commonest SRAM cell comprises two inverters and two n-channel pass transistors.

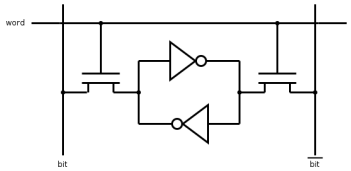

Figure 3: SRAM cell

   e) Why are nMOS FETs used in preference to pMOS FETs for the pass transistors? (2 marks)

   f) The back-to-back inverters in the SRAM cell sometimes have to be driven by a write operation and the stored state changed. This involves connecting two gate outputs together, normally an 'illegal' operation. Why can this work in this circumstance? (2 marks)

   g) Why would you normally model a block of SRAM at a *behavioural* level for purposes of simulation in (for example) Verilog? (2 marks)

3. a) With respect to ASIC design, define the terms: (3 marks)

   i. 'Critical Path',
   ii. 'Slack'
   iii. 'Static Timing Analysis' (STA)?

   b) Briefly explain how a CAD STA tool works. (3 marks)

   c) If the circuit has a target design operating frequency of 100 MHz what would be the maximum critical path if (naïvely) pragmatic engineering details are omitted? In practice, what sort of 'pragmatic engineering details' would affect the calculation and in what (qualitative) way should the comparison be altered? (3 marks)

   Designers can specify a target clock frequency as a *constraint* to the logic synthesizer. It is quite usual for the synthesizer to fail to meet the constraint initially; however there are techniques which can be applied automatically which *may* be able to alleviate this problem.

   d) Briefly describe two approaches which can be applied during logic synthesis to try to meet a challenging timing constraint, missed in a first, trial synthesis. (6 marks)

   e) In an SoC design you have a functional logic block 'bought in' from an outside contractor which you can't modify: it was quite expensive IP and already paid for: unfortunately, it's 5% slower that a timing target you *must* meet. Suggest how you might meet your goals in a cost-effective way, briefly justifying your solution. (5 marks)

END OF EXAMINATION